REMARKS

This is intended as a full and complete response to the Office Action dated October 3, 2006, (hereinafter "the Office Action") having a shortened statutory period for response set to expire on January 3, 2007.

Claims 8, 10-12, 15, and 20 have been amended. Claim 9 has been cancelled without prejudice. Support for the amendments may be found in the specification, for example at paragraphs [0026]-[0033], and thus no new matter is added by these amendments.

Claims 1-7 and 21-25 have been withdrawn with traverse. Applicants hereby withdraw the traversal with respect to the restriction requirement prompting the election of claims 8-20. Accordingly, claims 1-7 and 21-25 are withdrawn without traverse subject to the reservation of rights in the election.

Claim 20 was rejected under 35 U.S.C. § 112 as being indefinite. Claim 20 has been amended to overcome this rejection.

Claims 8-20 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,941,433 ("Libby"). With this rejection, Applicants respectfully disagree, at least for the reasons set forth below.

In Libby, latency is measured by having previously written a data pattern to a predetermined address and then sending a read request to such predetermined address while starting a latency measuring counting. (Libby, at col. 4, lines 57-65.) The number of clock cycles until the data pattern is received by a read FIFO and then clocked out of such read FIFO responsive to a return clock for input to a read latency detector is the latency. (Id.) Accordingly, this indicates an overall latency for the read data path between two integrated circuits. In Libby, this overall latency may be checked from time to time, and any such overall latency may be used as part of synchronization. (Libby, at col. 4, line 65, to col. 5, line 6.)

Additionally, Libby provides no check as to whether the RAM is operating within a latency parameter thereof. Whatever latency exists for the RAM is part of the overall latency measured by Libby. Moreover, in FIG. 2 of Libby, there is no write enable signal provided to the read FIFO. Rather, Libby clocks in data from RAM to the read

FIFO responsive to the return clock, and uses high frequency pointers adjusted for overall latency to output data from the read FIFO.

In contrast to Libby, amended claim 8 recites the feature of a delay compensation circuit including a counter configured to count responsive to clock pulses to track latency of a second integrated circuit and configured to reset a count responsive to a latency parameter of the second integrated circuit. In other words, an overall latency is not being determined as in Libby. Thus, no data pattern need be written to and read back from memory as in Libby. Rather, it is determined whether a latency parameter of the second integrated circuit has been met to determine a period of data validity. Along those lines, amended claim 8 recites the feature of the count being for establishing a period of data validity of a data signal.

Furthermore, with reference to amended claims 10 and 11, Libby does not have a loopback trace from a send portion to a receive portion of a first integrated circuit. Libby does not approximate propagation delay as claimed for example in claim 11 by use of a loopback trace. Rather, Libby includes propagation delay in an undifferentiated overall measured latency.

As part of the undifferentiated latency, Libby counts clock cycles until receipt by a read latency detector of a data pattern. Thus, Libby does not as part of the overall latency differentiate as to whether the memory is operating within a threshold latency. In contrast to Libby, amended claim 12 recites the feature of a counter configured to count down to zero starting from the latency parameter of the second integrated circuit prior to resetting.

Additionally, in contrast to Libby, amended claim 20 recites the feature of the first integrated circuit including at least one storage device coupled to receive a write enable signal, where the write enable signal is provided responsive to output of a receive portion of the first integrated circuit. Libby allows all data from RAM to be written to a read FIFO responsive to a return clock. Thus, Libby does not write enable the read FIFO only after a period of data validity has been reached.

Accordingly, it is respectfully submitted that features of amended claims 8, 10-12, and 20 are not shown or described by Libby, and thus Applicants believe that claims 8, 10-12, and 20 should be allowed. Additionally, Applicants believe that claims

13-19, which depend upon one or more respective allowable claims, should likewise be allowed.

CONCLUSION

All claims are in condition for allowance and a Notice of Allowance is respectfully requested. If there are any questions, the Applicants' attorney can be reached at Tel: 408-879-6149.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on December 20, 2006.

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